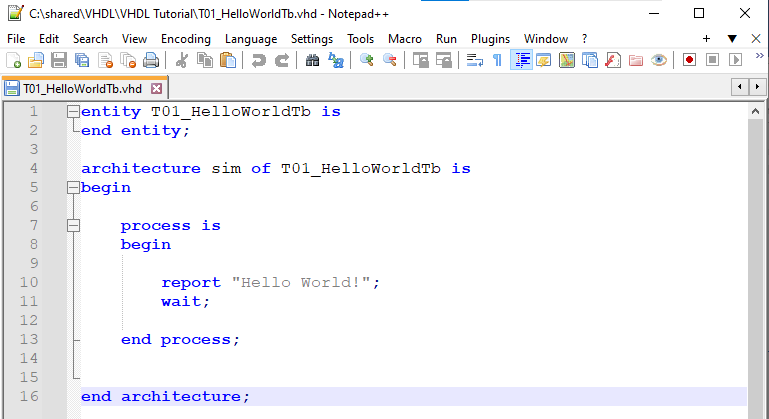
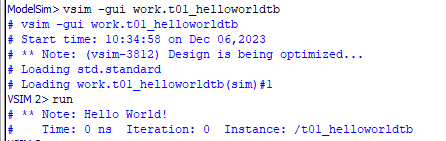
**VHDL Practice Code**

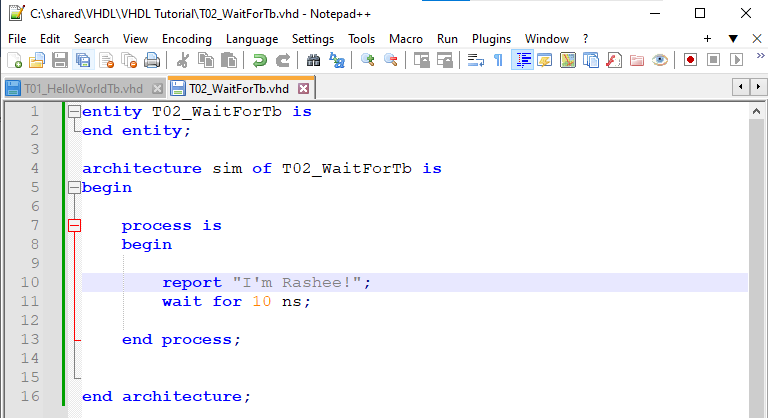
# **HelloWorld**



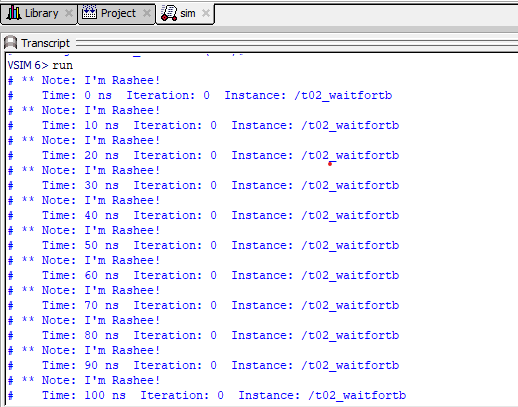
This print Hello World here no input or output



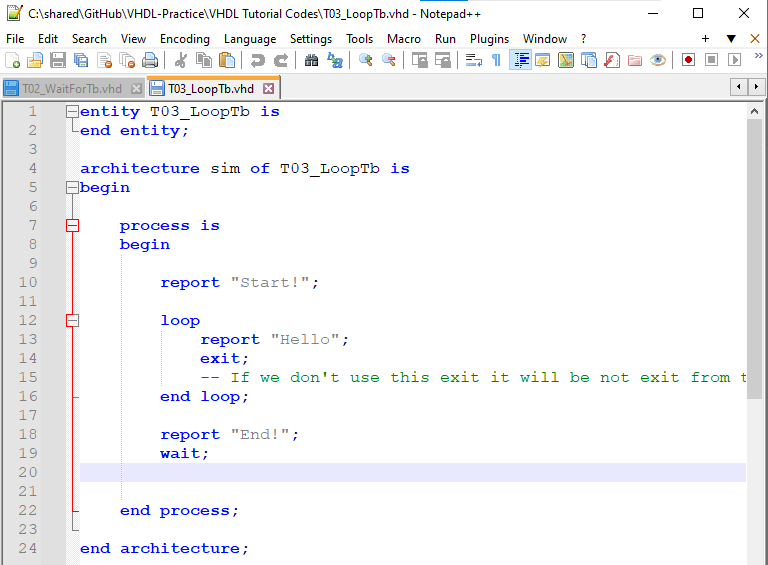
# **WaitFor**

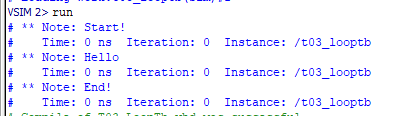


This is run in every 10 ns and we can set the simulation run time also by default is 100 ns.



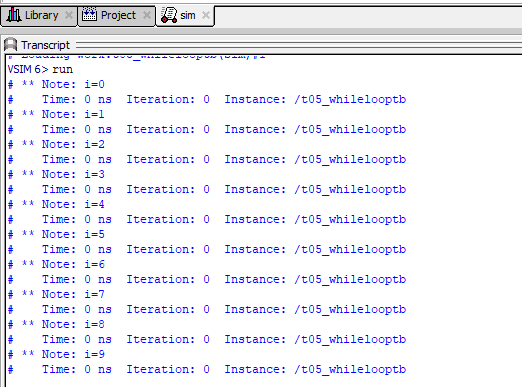
# **Loop**



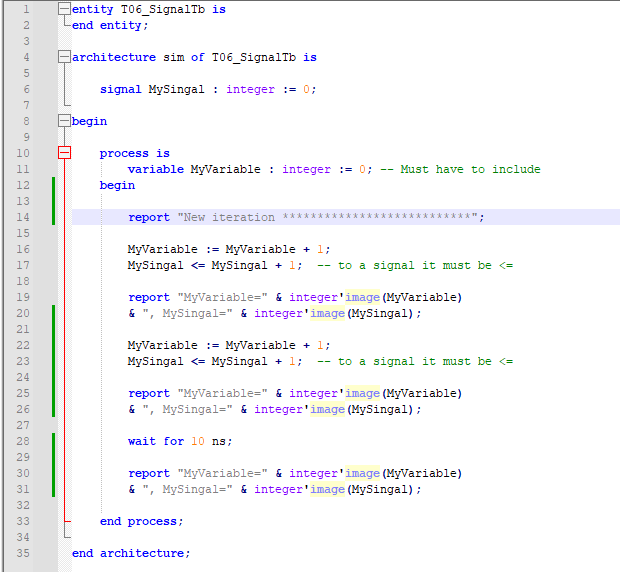


# **For loop**

# **While loop**

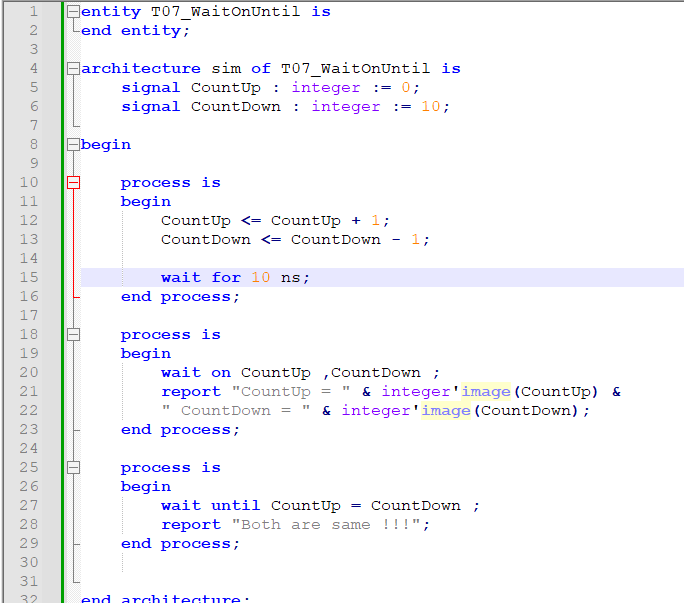


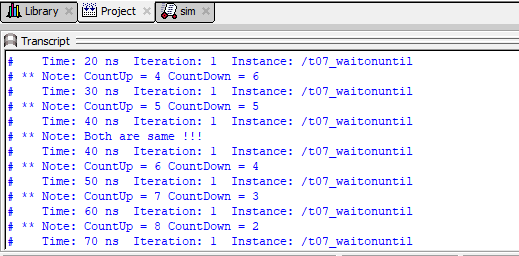
# **Signal**



Signals are update after the wait command and variables update with every operation

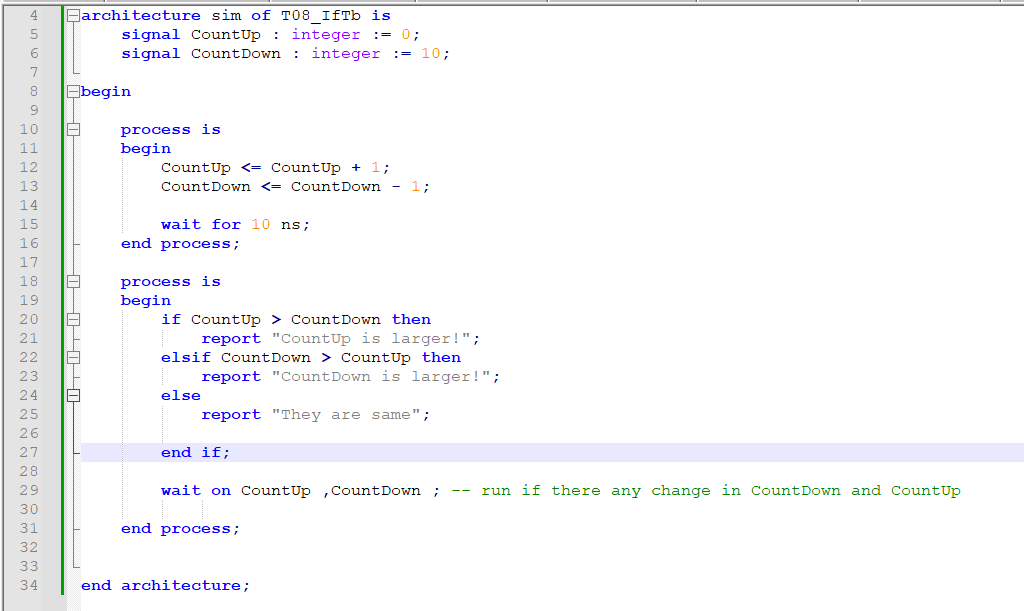
# **Wait on, Until**





Wait on run if there is any change in signals

# **If statement**



# **Sensitivity List**

# 

Both processes are taken same time

# **Std Logic**

